

FIG. 1

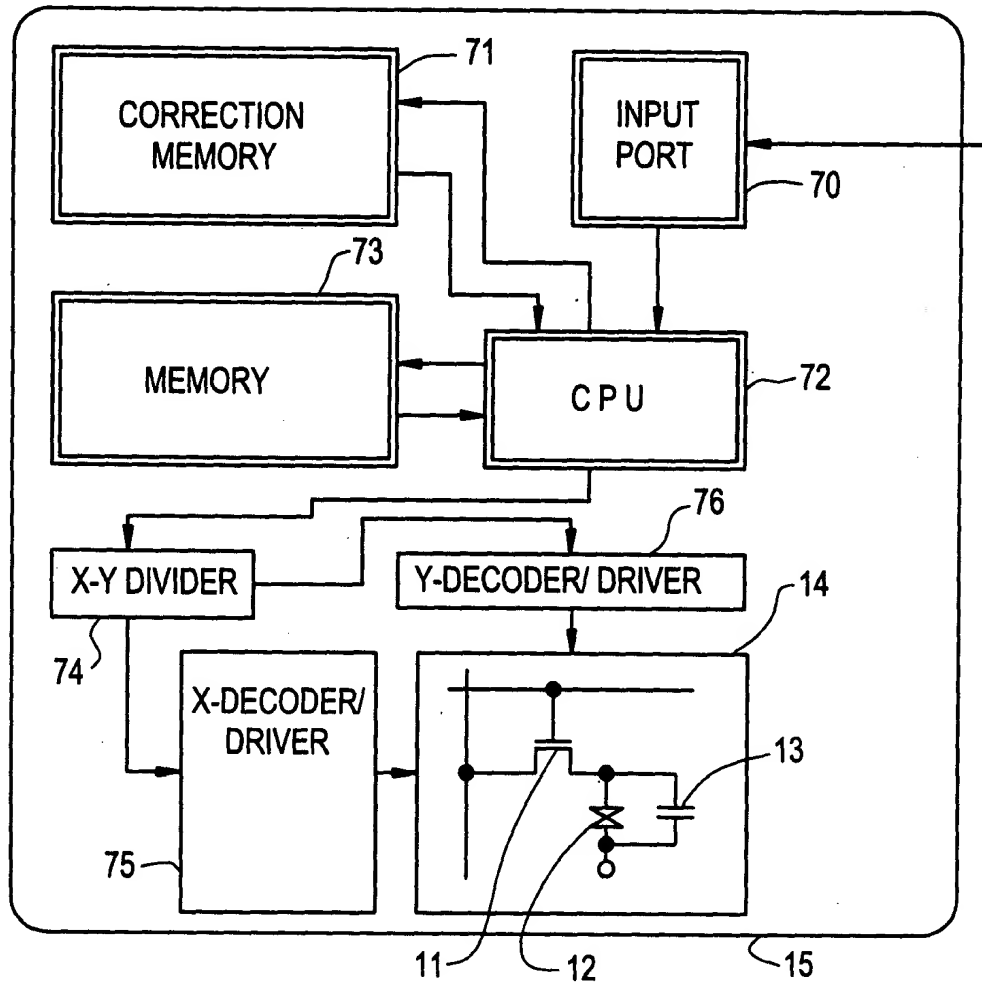


FIG. 2

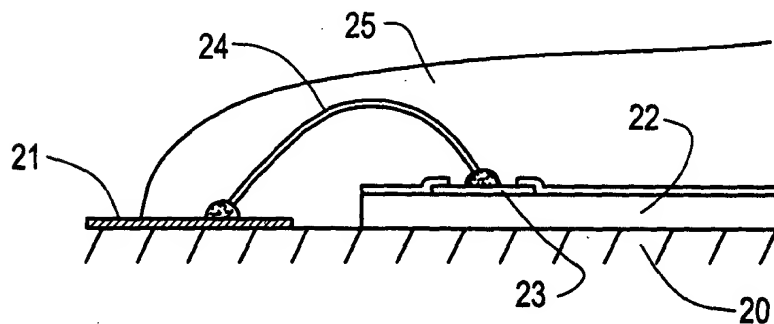


FIG. 3A

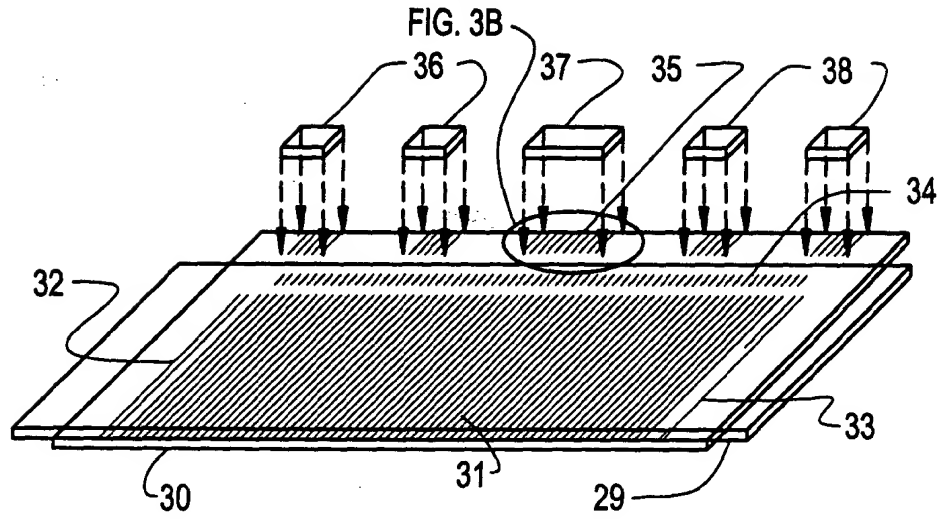


FIG. 3B

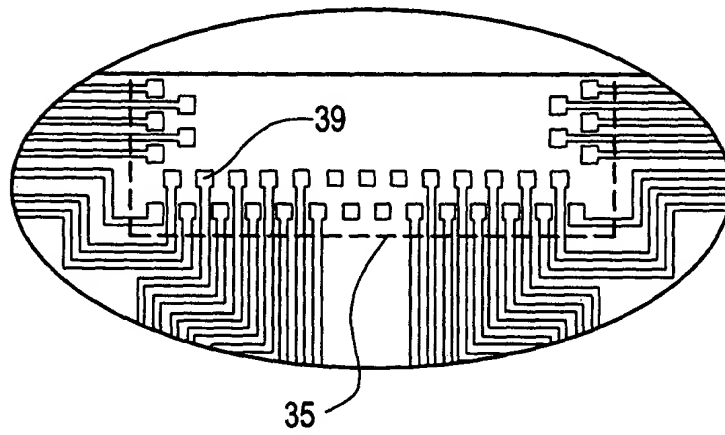


FIG. 4A

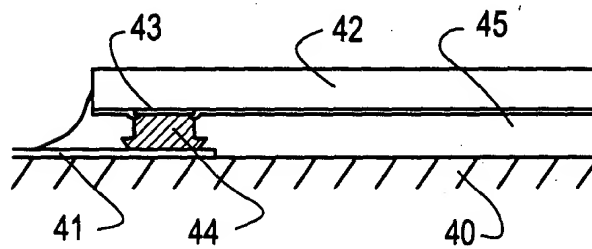


FIG. 4B

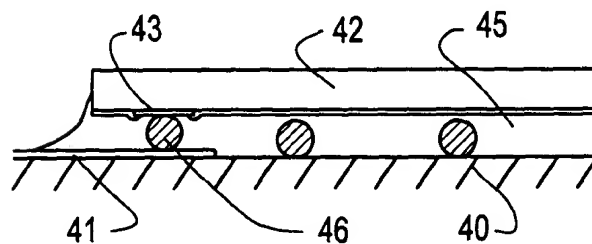


FIG. 5A

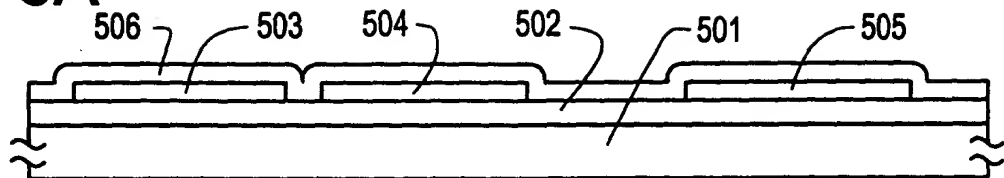


FIG. 5B

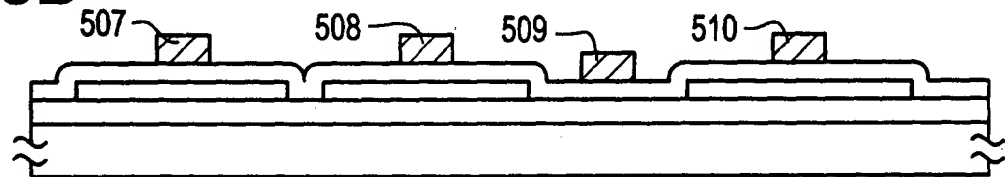


FIG. 5C

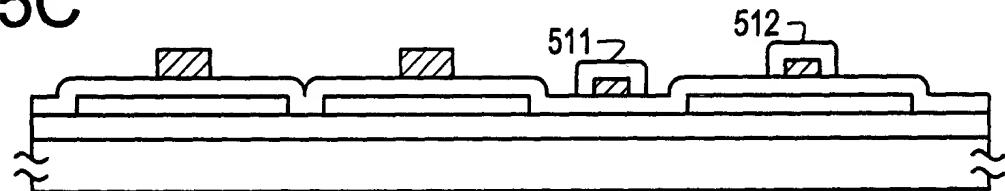


FIG. 5D

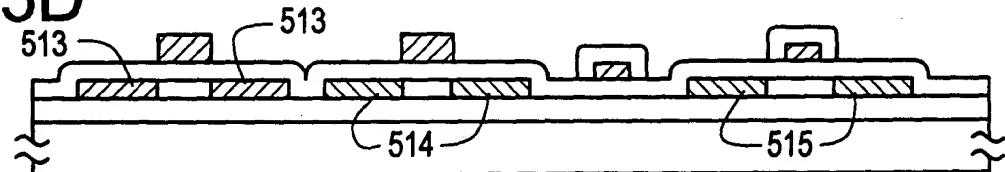


FIG. 5E

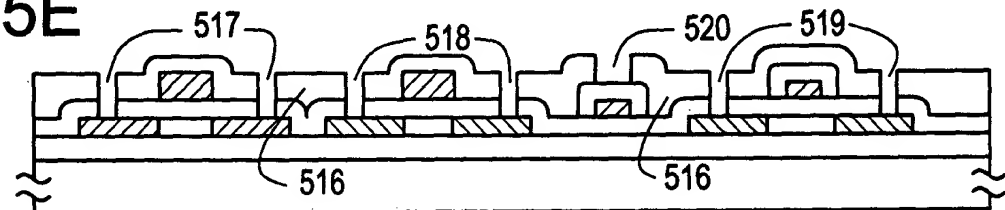


FIG. 5F

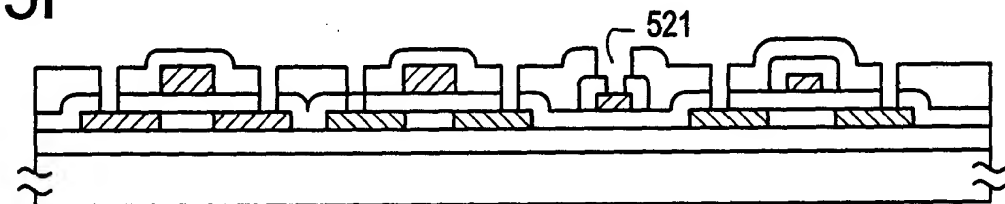


FIG. 5G

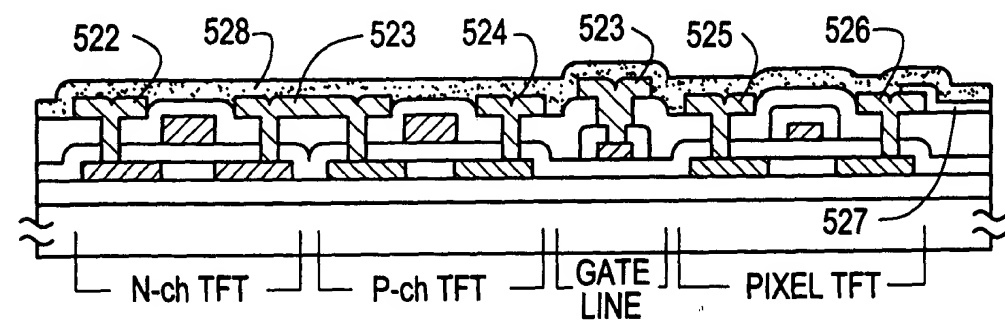


FIG. 6A

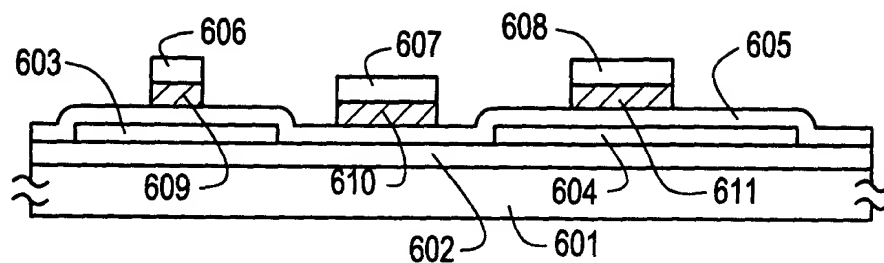


FIG. 6B

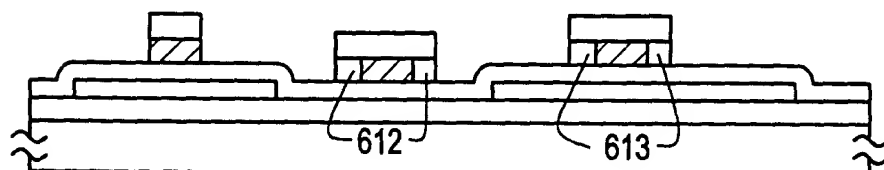


FIG. 6C

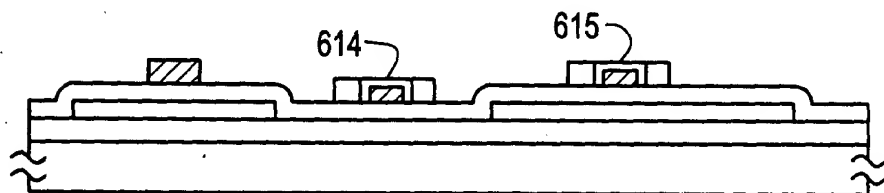


FIG. 6D

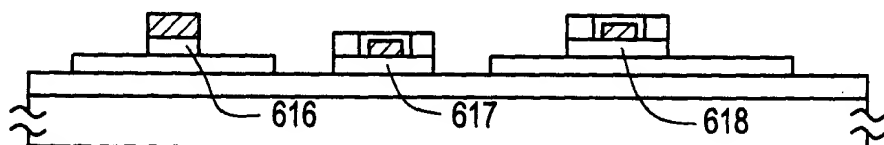


FIG. 6E

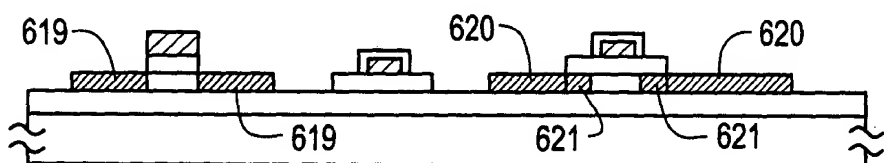


FIG. 6F

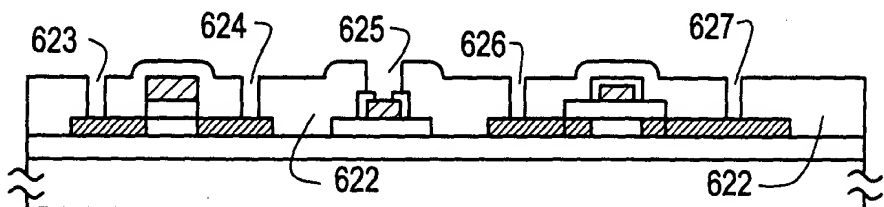


FIG. 6G

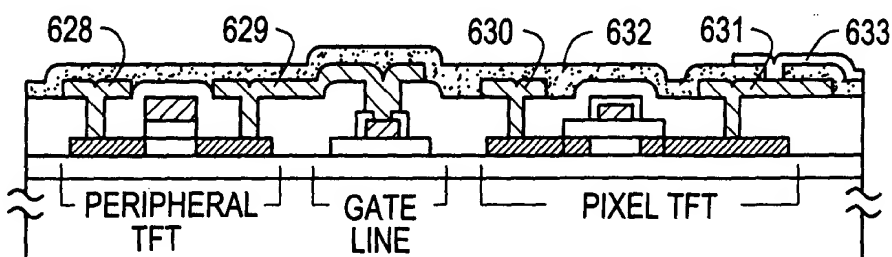


FIG. 7A

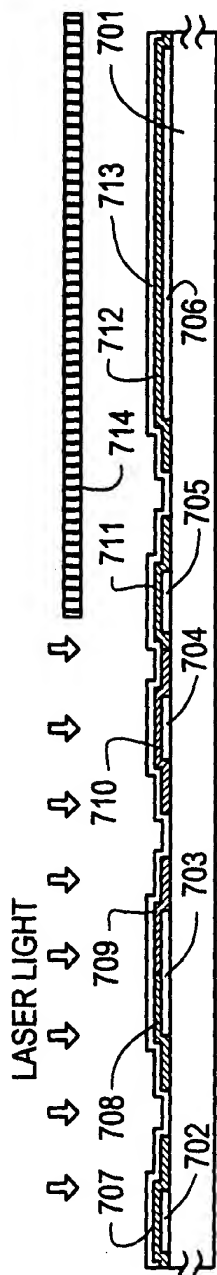


FIG. 7B

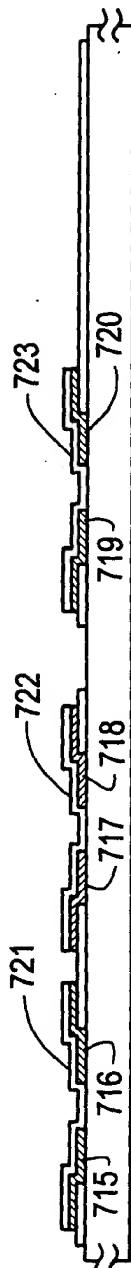


FIG. 7C

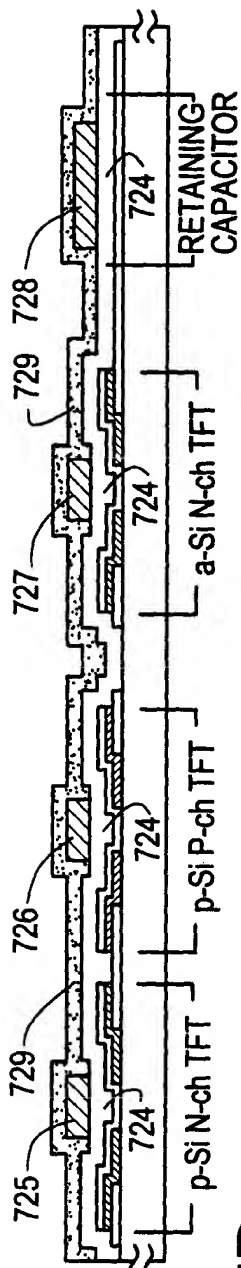


FIG. 7D

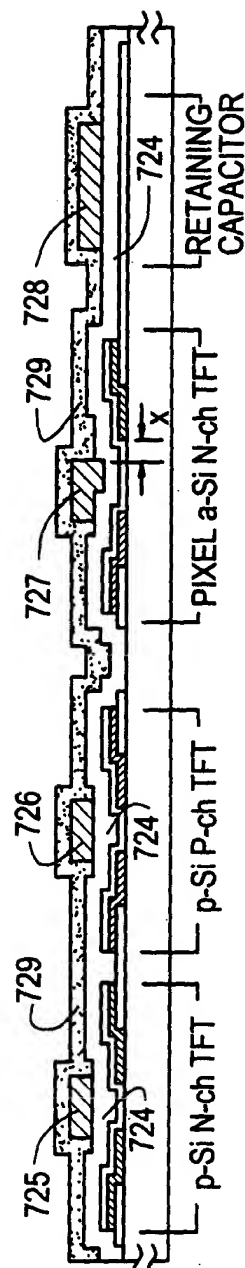


FIG. 8A

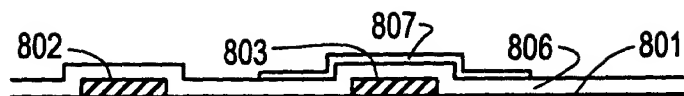


FIG. 8B

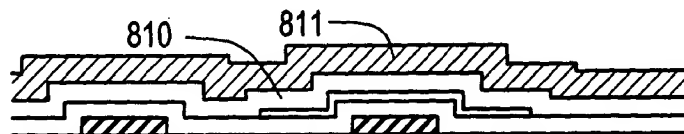


FIG. 8C

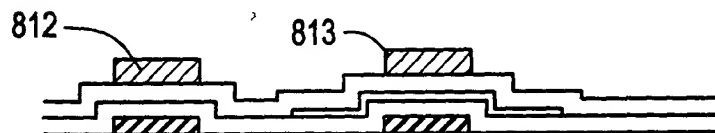


FIG. 8D

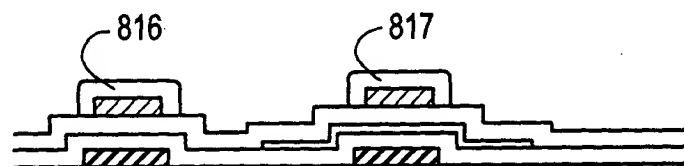


FIG. 8E

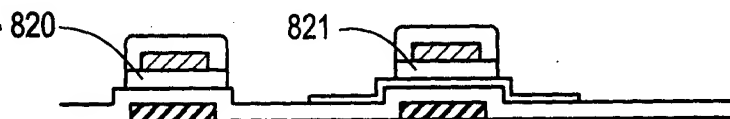


FIG. 8F



FIG. 8G



FIG. 8H

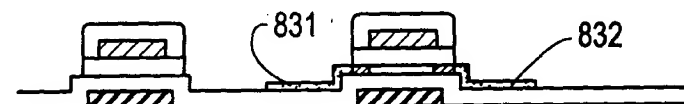


FIG. 8I

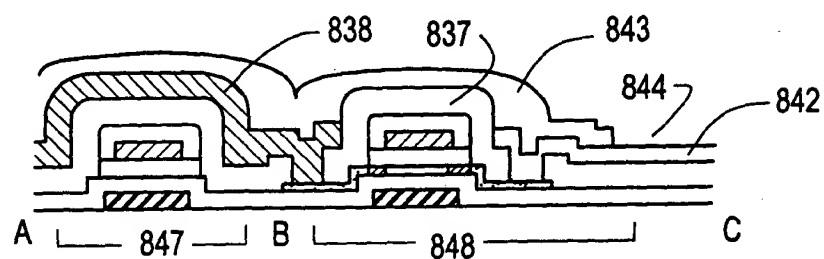


FIG. 9A

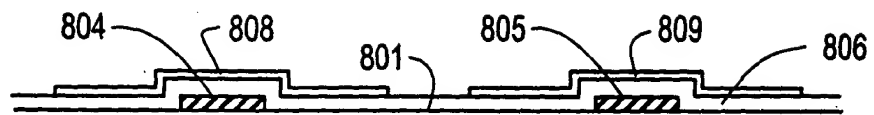


FIG. 9B

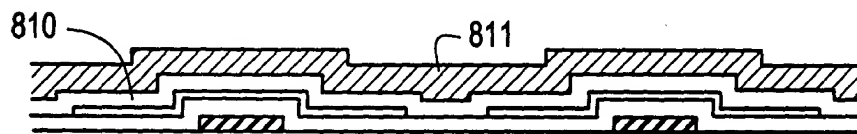


FIG. 9C



FIG. 9D



FIG. 9E

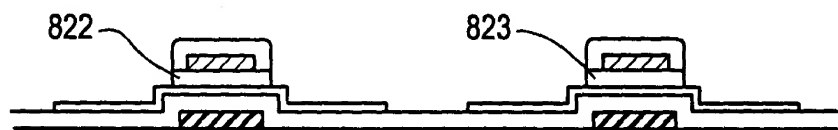


FIG. 9F

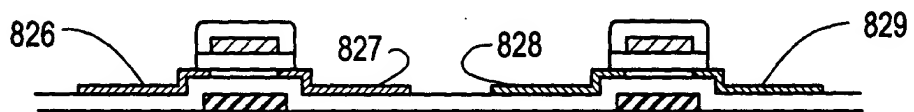


FIG. 9G

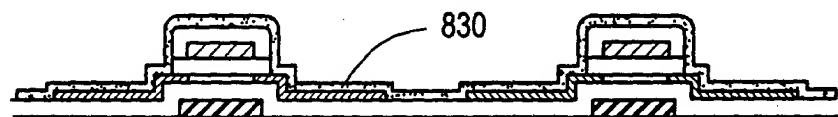


FIG. 9H

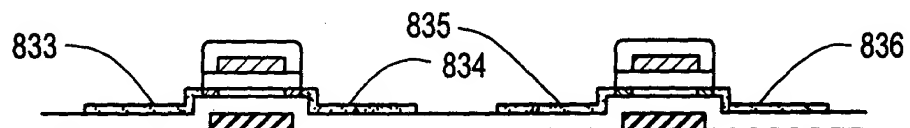


FIG. 9I

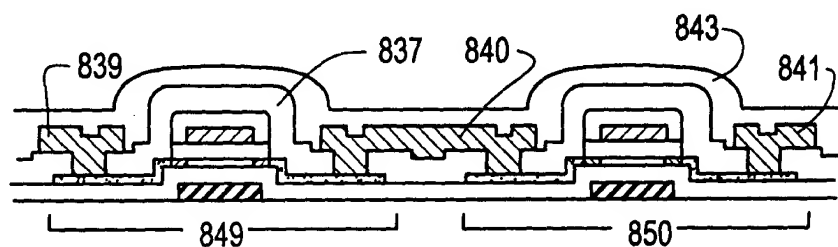


Figure 1 is a schematic diagram of a semiconductor device, specifically a memory array. It shows a 3x3 grid of memory cells. The array is defined by four horizontal lines (812, 803, 845, 838) and four vertical lines. Each cell contains a transistor (813) and a storage capacitor (846). A circled node is labeled 802.

FIG. 11A

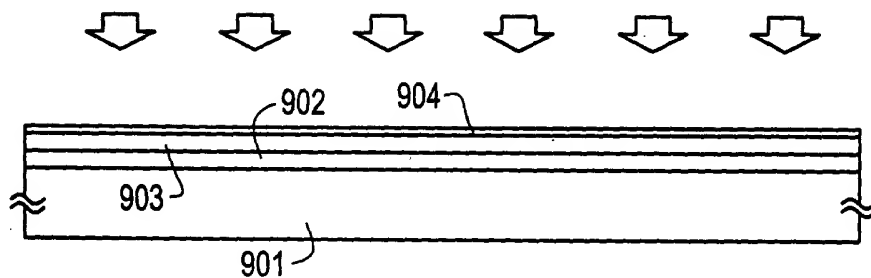


FIG. 11B

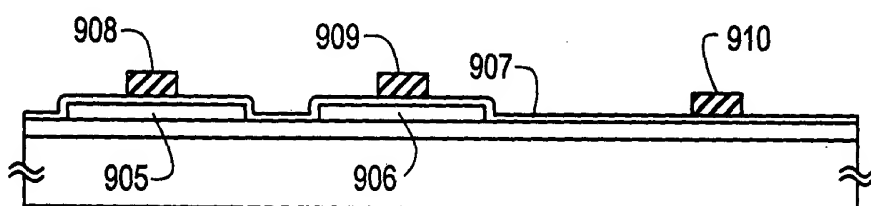


FIG. 11C

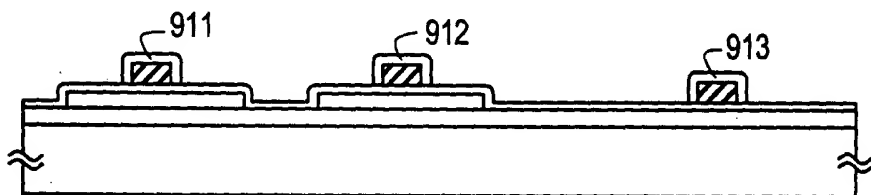


FIG. 11D

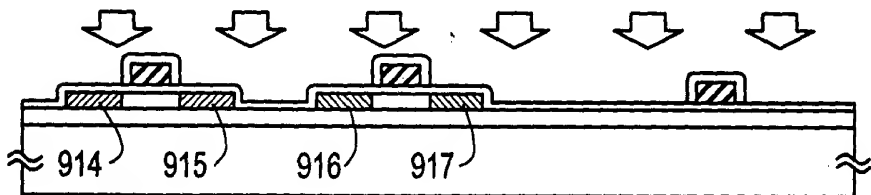


FIG. 11E

